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EXAMINER	
RAINEY, ROBERT R	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/705,775	MAEDA ET AL.	
	Examiner	Art Unit	
	ROBERT R. RAINEY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *13Feb2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01 February 2008 has been entered.

Response to Arguments

1. Applicant's arguments filed 01 February 2008 have been fully considered but they are not persuasive.

2. Applicant argues that the amendments to claim 11 overcome the objection to claim 18. Examiner disagrees. The amendments do not address the issue. The objection is maintained. The objection is repeated below.

3. Applicant notes that claim 11 was amended and that the rejections should be considered in light of the amendment. The only claim amended is claim 11. The amendments to claim 11 are such that the claim is broadened rather than narrowed. The amendments, consisting of the removal of a word and a phrase, do not serve to distinguish the claim or its dependents over the prior art. The rejection of claim 11 as formulated in the previous office action applies equally to claim 11 as amended.

Therefore, the rejections of claims 1-19 as made in the previous office action are maintained. The rejections as made in the previous office action are repeated below.

4. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., that the sampling timing of the video signal in each data signal line does not change) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

5. Applicant further argues that Sunao does not use a multiphased image signal, but the teaching of a multiphased image signal in Sunao was clearly set out in the previous office action. If by the phrase "it is impossible to use a multiphased image signal as claimed", Applicant means to imply some special multiphasing beyond that recited in the claims, then this would again be an argument concerning limitations not found in the claims since mapping of the teachings of Sunao to the claims in the prior office action indicates that the limitations as claimed are indeed taught.

6. Finally applicant argues that the deficiencies pointed out for the rejection of the claims over Sunao cause the rejections of their various dependent claims based on combinations of art including Sunao to be similarly deficient. Since, the argued deficiencies of Sunao have been refuted above the deficiencies of the rejections of the other claims are also refuted.

Claim Objections

7. **Claim 18** is objected to because of the following informalities:

Claims 18 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 18 states that "... data signal line groups are data signal line sets ...". There is no patentably distinct difference between the terms "groups" and "sets" in the context of the claim. Claim 18 does go on to define a data signal line set as "... made up of a predetermined number of the data signal lines corresponding to color signals contained in the video signal ...". Claim 11, as amended, defines a data signal line group as "comprising a predetermined number of adjacent data signal lines sequentially connected to each divisional video signal line so as to respectively correspond to the color signals". The definition given in claim 11 is narrower than the definition given in claim 18. Thus, neither the change of terminology from groups to sets nor the new definition given further limits claim 11. Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. **Claims 1, 2, 3, 4, 7, 10, 11, 12, 15, 18, 19, and 21** are rejected under 35 U.S.C. 102(b) as being anticipated by Japanese Patent Application No. *JP2000-181394* ("*Sunao*").

Regarding **Claim 1**, *Sunao* discloses a data signal line driving method for driving a plurality of data signal lines (for example, "S1-S4n" in Fig 1 and paragraph 0025) respectively so as to fetch (see for example, Fig 1 sampling circuit 130, switch 131, decoder 140 and sampling signals X1...X4 with operation described in Figs 4-7, 9 and 10) a multiphased video signal (for example, "V1-Vn" in Figs 4-7, 9, and 10) via a plurality of video signal lines (for example, "V1-Vn" in Fig 1 and paragraph 0025) into the data signal lines, said method comprising the steps of: gathering data signal line groups, each group comprising a predetermined number of adjacent data signal lines sequentially connected to each video signal line (for example 4 data signal lines, i.e. S1-S4 to V1, S4-S8 to V2, ... S4(n-3)-S4(n) to Vn, are shown sequentially connected to each video signal line in Fig 1), the predetermined number of adjacent data signal lines being equal to the number of the video signal lines (see for example Fig. 1 with n=4), a number of data signal line groups equal to the number of video signal lines being regarded as a single block (data signal line groups 1-n are "gathered" that is treated as a single block see for example Figs 4-7, 9, or 10); and fetching

the video signal from the video signal lines into the data signal lines in each block (see for example Figs 4-7, 9, or 10).

Regarding **Claim 2**, *Sunao* discloses a data signal line driving method for driving a plurality of data signal lines (see for example Fig 12) respectively so as to (i) multiphase a video signal having a plurality of color signals (see for example VG1,VB1,VR1 ... of Fig 12) and (ii) fetch the video signal into the data signal lines, said method comprising the steps of: causing a plurality of divisional video signal lines, divided so as to respectively correspond to the color signals, to constitute each of the video signal lines ("V1-Vn" in Fig 1 and paragraph 0025 as modified by Fig 12 and paragraph 0101); gathering data signal line groups, each group comprising a predetermined number of adjacent data signal lines sequentially connected to each divisional video signal line so as to respectively correspond to the color signals (for example, 4 data signal lines, i.e. S1-S4 to V1, S4-S8 to V2, ... S4(n-3)-S4(n) to Vn, are shown sequentially connected to each video signal line in Fig 1 and Fig 12 and paragraph 0101 extend this to color signals), the predetermined number of adjacent data signal lines being equal to the number of the video signal lines (see for example Fig. 1 with n=4 as modified by Fig 12 and paragraph 0101), said data signal line group being regarded as a single block (for example, data signal line groups 1-n are "gathered" that is treated as a single block as shown in Figs 4-7, 9, and 10 and Fig 12 and paragraph 0101 extend this to color); and fetching the video signal from the video

signal lines into the data signal lines in each block (see for example Fig 1 sampling circuit 130, switch 131, decoder 140 and sampling signals X1…X4 with operation described in Figs 4-7, 9 and 10 expanded to color by Fig 12 and paragraph 0101).

Regarding **Claim 3**, *Sunao* discloses a data signal line driving circuit, which drives a plurality of data signal lines (see for example "S1-S4n" in Fig 1 and paragraph 0025) respectively so as to fetch (see for example Fig 1 sampling circuit 130, switch 131, decoder 140 and sampling signals X1…X4 with operation described in Figs 4-7, 9) a multiphased video signal (see for example "V1-Vn" in Figs 4-7, 9, and 10) via a plurality of video signal lines into the data signal lines, comprising: data signal line groups, each group comprising a predetermined number of adjacent data signal lines sequentially connected to each video signal line (see for example that 4 data signal lines, i.e. S1-S4 to V1, S4-S8 to V2, … S4(n-3)-S4(n) to Vn, are shown sequentially connected to each video signal line in Fig 1); and a video signal fetching section (see for example Fig 1 sampling circuit 130, switch 131, decoder 140 and sampling signals X1…X4) for fetching the video signal from the video signal lines into the data signal lines in each block when gathering data signal line groups, each group comprising a predetermined number of adjacent data signal lines sequentially connected to each video signal line (see for example that 4 lines, i.e. S1-S4 to V1, S4-S8 to V2, … S4(n-3)-S4(n) to Vn, are shown sequentially connected to each video signal line in Fig 1), the

predetermined number of adjacent data signal lines being equal to the number of the video signal lines (see for example Fig. 1 with n=4), a number of data signal line groups equal to the number of video signal lines being regarded as a single block (data signal line groups 1-n are "gathered" that is treated as a single block see for example Figs 4-7, 9, or 10).

Regarding **Claims 4 and 7**, *Sunao*, in addition to the rejection of claim 3, discloses that the video signal fetching section includes drive switching means (claim 3) or a drive switching circuit (claim 7) for switching between (i) first driving in which the data signal lines of one of the data signal line groups in the block and the data signal lines of another one of the data signal line groups in the block are driven at the same time and (ii) second driving in which all the data signal lines of the data signal line groups are driven at the same time (Fig 1 decoder 140 and sampling signals X1, X2, X3, X4 allow any combination of the four sampling switches 131 in each data signal line group to sample the group's respective video signal clearly covering one per data signal line group and all signal lines in the signal line groups. Fig 6 illustrates all signal lines in the groups sampling at the same time. Both modes i and ii are covered by all signal lines sampling at the same time because mode i says that one and another data signal line groups in a block, i.e. at least two data signal line groups in a block, are driven at the same time and mode ii says that all data signal line groups are driven at the same time.).

Regarding **Claim 10**, *Sunao*, in addition to the rejection of claim 3, discloses that the data signal line groups are data signal line sets each of which is made up of a predetermined number of data signal lines respectively corresponding to color signals contained in the video signal fetched into the data signal lines (Fig 1 and paragraph 0028 as extended to color by Fig 12 and paragraph 0101).

Regarding **Claim 11**, *Sunao* discloses a data signal line driving circuit, which drives a plurality of data signal lines respectively so as to (i) multiphase a video signal having a plurality of color signals (see for example VG1,VB1,VR1 etc. of Fig 12) and (ii) fetch the video signal into the data signal lines, comprising: a plurality of divisional video signal lines, divided so as to respectively correspond to the color signals, which constitute each of the video signal lines ("V1-Vn" in Fig 1 and paragraph 0025 as modified by Fig 12 and paragraph 0101); and a video signal fetching section (Fig 1 sampling circuit 130, switch 131, decoder 140 and sampling signals X1...X4 with operation described in Figs 4-7, 9 and 10 expanded to color by Fig 12 and paragraph 0101) for fetching the video signal from the video signal lines into the data signal lines in each block when gathering data signal line groups, each group comprising a predetermined number of adjacent data signal lines ~~sequentially~~ (Note: the words deleted by the most recent amendment are shown in strikethrough for reference.) connected to

each divisional video signal line ~~so as to respectively correspond to the color signals~~ (for example, 4 data signal lines, i.e. S1-S4 to V1, S4-S8 to V2, ... S4(n-3)-S4(n) to Vn, are shown sequentially connected to each video signal line in Fig 1 and Fig 12 and paragraph 0101 extend this to color signals), the predetermined number of adjacent data signal lines being equal to the number of the video signal lines (see for example Fig. 1 with n=4 as modified by Fig 12 and paragraph 0101), said data signal line group being regarded as a single block (see for example that data signal line groups 1-n are "gathered" that is treated as a single block as shown in Figs 4-7, 9, and 10 and Fig 12 and paragraph 0101 extend this to color).

Regarding **Claims 12 and 15**, *Sunao*, in addition to the rejection of claim 11, discloses that the video signal fetching section includes drive switching means (claim 12) or a drive switching circuit (claim 15) for switching between (i) first driving in which the data signal lines of one of the data signal line groups in the block and the data signal lines of another one of the data signal line groups in the block are driven at the same time and (ii) second driving in which all the data signal lines of the data signal line groups are driven at the same time (Fig 1 decoder 140 and sampling signals X1, X2, X3, X4 allow any combination of the four sampling switches 131 in each data signal line group to sample the group's respective video signal clearly covering one per data signal line group and all signal lines in the signal line groups. Fig 6 illustrates all signal lines in the groups

sampling at the same time. Both modes i and ii are covered by all signal lines sampling at the same time because mode i says that one and another data signal line groups in a block, i.e. at least two data signal line groups in a block, are driven at the same time and mode ii says that all data signal line groups are driven at the same time.).

Regarding **Claim 18**, *Sunao*, in addition to the rejection of claim 11, discloses that the data signal line groups are data signal line sets each of which is made up of a predetermined number of the data signal lines corresponding to color signals contained in the video signal fetched into the data signal lines (see for example Fig 1 and paragraph 0028 as extended to color by Fig 12 and paragraph 0101).

Regarding **Claim 19**, *Sunao* discloses a display device, comprising: a display panel (paragraph 0105 and Figs. 13 and 14) which includes (i) a plurality of data signal lines ("S1-S4n" in Fig 1 and paragraph 0025), (ii) a plurality of scanning signal lines provided so as to cross the data signal lines (G1 to Gm in Fig 1 and paragraph 25), and (iii) pixels provided on intersections of the data signal lines and the scanning signal lines (118 in Fig 1 and paragraph 0025), a video signal for displaying an image being fetched from the data signal lines into the pixels in synchronism with a scanning signal supplied from the scanning signal lines (Figs. 1 and 4 and paragraph 0033), said video signal being retained

(paragraph 0036 describes "a picture signal…written in a pixel"); a data signal line driving circuit for outputting the video signal to the data signal lines in synchronism with a predetermined timing signal (Figs. 1 and 4 and paragraph 0036); and a scanning signal line driving circuit for outputting the scanning signal to the scanning signal lines in synchronism with a predetermined timing signal (Figs. 1 and 4 and paragraph 0033), said video signal being multiphased ("V1-Vn" in Figs 4-7, 9, and 10), and being supplied to the data signal lines via a plurality of video signal lines ("V1-Vn" in Fig 1 and paragraph 0025), wherein the data signal line driving circuit, which drives said plurality of data signal lines respectively so as to fetch the multiphased video signal via said plurality of video signal lines into the data signal lines, includes: data signal line groups, each group comprising a predetermined number of adjacent data signal lines sequentially connected to each video signal line (see for example that 4 data signal lines, i.e. S1-S4 to V1, S4-S8 to V2, … S4(n-3)-S4(n) to Vn, are shown sequentially connected to each video signal line in Fig 1); and a video signal fetching section (see for example Fig 1 sampling circuit 130, switch 131, decoder 140 and sampling signals X1…X4) for fetching the video signal from the video signal lines into the data signal lines in each block when gathering data signal line groups, each group comprising a predetermined number of adjacent data signal lines sequentially connected to each video signal line (see for example that 4 lines, i.e. S1-S4 to V1, S4-S8 to V2, … S4(n-3)-S4(n) to Vn, are shown sequentially connected to each video signal line in Fig 1), the predetermined

number of adjacent data signal lines being equal to the number of the video signal lines (see for example Fig. 1 with n=4), a number of data signal line groups equal to the number of video signal lines being regarded as a single block (data signal line groups 1-n are "gathered" that is treated as a single block see for example Figs 4-7, 9, or 10).

Regarding **Claim 21**, *Sunao* discloses a display device, comprising: a display panel (paragraph 0105 and Figs. 13 and 14) which includes (i) a plurality of data signal lines ("S1-S4n" in Fig 1 and paragraph 0025), (ii) a plurality of scanning signal lines provided so as to cross the data signal lines (G1 to Gm in Fig 1 and paragraph 25), and (iii) pixels provided on intersections of the data signal lines and the scanning signal lines (118 in Fig 1 and paragraph 0025), a video signal for displaying an image being fetched from the data signal lines into the pixels in synchronism with a scanning signal supplied from the scanning signal lines (Figs. 1 and 4 and paragraph 0033), said video signal being retained (paragraph 0036 describes "a picture signal...written in a pixel"); a data signal line driving circuit for outputting the video signal to the data signal lines in synchronism with a predetermined timing signal (Figs. 1 and 4 and paragraph 0036); and a scanning signal line driving circuit for outputting the scanning signal to the scanning signal lines in synchronism with a predetermined timing signal (Figs. 1 and 4 and paragraph 0033), said video signal being multiphased ("V1-Vn" in Figs 4-7, 9, and 10), and being supplied to the data signal lines via a

plurality of video signal lines ("V1-Vn" in Fig 1 and paragraph 0025 as modified by Fig 12 and paragraph 0101), wherein the data signal line driving circuit, which drives a plurality of data signal lines respectively so as to (a) multiphase the video signal having a plurality of color signals and (b) fetch the video signal into the data signal lines, includes: a plurality of divisional video signal lines, divided so as to respectively correspond to the color signals, which constitute each of the video signal lines ("V1-Vn" in Fig 1 and paragraph 0025 as modified by Fig 12 and paragraph 0101); and a video signal fetching section (Fig 1 sampling circuit 130, switch 131, decoder 140 and sampling signals X1...X4 with operation described in Figs 4-7, 9 and 10 expanded to color by Fig 12 and paragraph 0101) for fetching the video signal from the video signal lines into the data signal lines in each block when gathering data signal line groups, each group comprising a predetermined number of adjacent data signal lines sequentially connected to each divisional video signal line so as to respectively correspond to the color signals (for example, 4 data signal lines, i.e. S1-S4 to V1, S4-S8 to V2, ... S4(n-3)-S4(n) to Vn, are shown sequentially connected to each video signal line in Fig 1 and Fig 12 and paragraph 0101 extend this to color signals), the predetermined number of adjacent data signal lines being equal to the number of the video signal lines (see for example Fig. 1 with n=4 as modified by Fig 12 and paragraph 0101), said data signal line group being regarded as a single block (see for example that data signal line groups 1-n are "gathered" that is treated as

a single block as shown in Figs 4-7, 9, and 10 and Fig 12 and paragraph 0101 extend this to color).

10. **Claims 5, 6, 8, 9, 13, 14, 16, 17, 20, and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over published Japanese Patent Application No. *JP2000-181394* ("*Sunao*") in view of applicants admitted prior art ("*APArt*") and *U.S. Patent No. 5,781,171 ("Kihara")*.

As to **claims 5 and 6**, in addition to the rejection of claim 4 over *Sunao*, *Sunao* further discloses the use of shift registers to generate timing signals very similar to those used for fetching video signals. Referring to Fig 4 of Sunao see the similarities between the timing pulses X1 and X2 that cause the video signals to be fetched from the video signal lines to the data signal lines and the signals G1 and G2 for the generation of which Sunao teaches the use of shift registers. Sunao further discloses drive switching means switches between the first driving and the second driving so that the number of the shift registers that operate is varied in switching between the first driving and the second driving and further stopping operation of the shift register which is not required in driving after switching the drive switching means between the first driving and the second driving (claim 6). (See paragraph 0014 in which is the teaching to "..stop that part and power consumption" referring to a shift register stage that is not needed because of a reduction in the number of required outputs when a lower resolution driving mode is selected.)

Sunao does not expressly disclose a video signal fetching section that includes one or more shift registers for generating a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines since Sunao limits specific mention of shift registers to generating scan line timing signals.

Kihara discloses the use of shift registers to control sampling of signals into data signal lines (see for example items 200, 210 and 260 of Fig. 1)

APArt discloses a video signal fetching section that includes one or more shift registers for generating a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines. See for example Figure 22.

Sunao and *APArt* are analogous art because they are from the same field of endeavor, which is video display and seek to solve the same problem, which is to reduce power consumption when switching from display of higher to lower-resolution video signals.

At the time of invention, it would have been obvious to a person of ordinary skilled in the art to modify *Sunao* according to the well known practice of using shift registers to generate a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines and to include means to vary the number of shift registers used and even stop the operation of unneeded shift registers according to the resolution as taught by *Sunao*. The suggestion/motivation would have been that given by *Sunao*, which is to lower the power consumption (see Abstract and paragraph 0014).

Claims 8 and 9, are identical to claims 5 and 6 except for the substitution of the word "circuit" for "means" ("drive switching circuit" in claims 8 and 9 versus "drive switching means" in claims 5 and 6) and are rejected using the same arguments as used for claims 5 and 6.

As to **claims 13 and 14**, in addition to the rejection of claim 12 over *Sunao*, *Sunao* further discloses the use of shift registers to generate timing signals very similar to those used for fetching video signals. Referring to Fig 4 of Sunao see the similarities between the timing pulses X1 and X2 that cause the video signals to be fetched from the video signal lines to the data signal lines and the signals G1 and G2 for the generation of which Sunao teaches the use of shift registers. Sunao further discloses drive switching means switches between the first driving and the second driving so that the number of the shift registers that operate is varied in switching between the first driving and the second driving and further stopping operation of the shift register which is not required in driving after switching the drive switching means between the first driving and the second driving (claim 14). (See paragraph 0014 in which is the teaching to "..stop that part and power consumption" referring to a shift register stage that is not needed because of a reduction in the number of required outputs when a lower resolution driving mode is selected.)

Sunao does not expressly disclose a video signal fetching section that includes one or more shift registers for generating a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines since Sunao limits specific mention of shift registers to generating scan line timing signals.

Kihara discloses the use of shift registers to control sampling of signals into data signal lines (see for example items 200, 210 and 260 of Fig. 1)

APArt discloses a video signal fetching section that includes one or more shift registers for generating a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines. See for example Figure 22.

Sunao and *APArt* are analogous art because they are from the same field of endeavor, which is video display and seek to solve the same problem, which is to reduce power consumption when switching from display of higher to lower-resolution video signals.

At the time of invention, it would have been obvious to a person of ordinary skilled in the art to modify *Sunao* according to the well known practice of using shift registers to generate a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines and to include means to vary the number of shift registers used and even stop the operation of unneeded shift registers according to the resolution as taught by *Sunao*. The suggestion/motivation would have been that given by *Sunao*, which is to lower the power consumption (see Abstract and paragraph 0014).

Claims 16 and 17, are identical to claims 13 and 14 except for the substitution of the word "circuit" for "means" ("drive switching circuit" in claims 16 and 17 versus "drive switching means" in claims 13 and 14) and are rejected using the same arguments as used for claims 13 and 14.

11. **Claims 20, and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over published Japanese Patent Application No. *JP2000-181394* ("*Sunao*") in view of *U.S. Patent No. 5,781,171 ("Kihara")*.

As to **claims 20 and 22**, in addition to the rejections of claims 19 and 21 respectively over *Sunao*:

Sunao does not expressly disclose the data signal line driving circuit, the scanning signal line driving circuit, and the pixels formed on the same substrate.

Kihara discloses the data signal line driving circuit, the scanning signal line driving circuit, and the pixels formed on the same substrate (see Fig. 1 and paragraphs at column 6 lines 31-34 and column 11 line 62 to column 12 line 5).

Sunao and *Kihara* are analogous art because they are from the same field of endeavor, which is display drive.

At the time of invention, it would have been obvious to a person of ordinary skilled in the art to modify the device described in *Sunao* such that the data signal line driving circuit, the scanning signal line driving circuit, and the

pixels are formed on the same substrate as taught by *Kihara*. The suggestion/motivation would have been to reduce cost. *Kihara* does not provide motivation directly for the integrated structure but refers to it as the "so-called driver integrated structure" (see column 6, line 32) implying that this type of structure is one of well known value. Since integrating multiple devices onto a single substrate is a well know way to reduce cost, one of ordinary skill in the art at the time of the invention would have recognized its value.

Conclusion

12. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT R. RAINEY whose telephone number is (571)270-3313. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/RR/

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